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May 26, 2004

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Applicants: Praveen K. Samudrala**

**Serial No.: 10/708,268**

**Filing Date: 02/20/2004**

**For: Method and Apparatus for Creating Circuit Redundancy in Programmable Logic Devices**

**Our Reference No.: 1372.136.PRC**

**Examiner: Unassigned**

**Art Unit: 2816**

Dear Sir:

Enclosed please find the following:

1. Information Disclosure Statement By Applicants- 1 page;
2. Copies of the front covers of five (5) Non-Patent Literature Documents; and
3. Self-addressed, postage prepaid post card to serve as a receipt for items 1-2.

Very respectfully,

**SMITH & HOPEN**

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AJH/cm  
enclosure

**CERTIFICATE OF MAILING**  
(37 C.F.R. 1.8)

I HEREBY CERTIFY that this correspondence is being mailed with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 26, 2004.

Date: May 26, 2004

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Complete if Known</b>	
		Application Number	10/708,268
		Filing Date	02/20/2004
		First Named Inventor	Praveen K. Samudrala
		Art Unit	2816
		Examiner Name	Unassigned
Sheet 1	of 1	Attorney Docket Number	1372.136.PRC

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	1	SAMUDRALA, PRAVEEN KUMER ET AL., Selective Triple modular Redundancy for SEU Mitigation in FPGAs, pgs 1-3.	
	2	SAMUDRALA, PRAVEEN K. ET AL., Selective Triple Modular Redundancy (STMR) Based Single Event Upset (SEU) Tolerant Synthesis for FPGAs, pgs 1-26.	
	3	SAMUDRALA, PRAVEEN K. ET AL., A Novel Technique for SEU Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31.	
	4	CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0).	
	5	LABEL, KENNETH A. ET AL., Single-Event-Effect Mitigation from a System Perspective, IEEE Transactions on Nuclear Science, April 1996, 46-2.	

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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